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EXAMINER	
VITAL, PIERRE M	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,800	NEUMAN, PAUL S.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed August 12, 2005 in response to PTO Office Action mailed May 10, 2005. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-25 have been presented for examination in this application. In response to the last Office Action, claims 1, 5, 8, 11 and 16 have been amended. No claims have been canceled or added. As a result, claims 1-25 remain pending in this application.

3. The rejection of claims 11-15 under 112, first paragraph has been withdrawn due to the amendment filed August 12, 2005.

Response to Arguments

4. Applicant's arguments, see Remarks, filed August 12, 2005, with respect to the rejection(s) of newly amended claim(s) 1-25 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made. Rejection of the claims based on the new grounds follow herewith.

5. Applicant's arguments filed August 12, 2005 have been fully considered but they are not persuasive. As to the remarks, applicant asserted that:

(b) There is no showing of the generation of a parity error by a level two cache memory in Hazawa.

Note that the level 0 cache of Hazawa is equivalent to the level 1 cache of the present invention and the level 1 cache of Hazawa is equivalent to the level 2 cache of the present invention and so forth. Also note that Hazawa discloses an error has occurred at level 1 cache (col. 3, lines 45-57). Invalidating can only be done at corresponding locations of the L1 and L2 caches since parity check is often used to check the accuracy with which each byte is stored. As such, Hazawa teaches the generation of a parity error by a level two cache memory.

(b) In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the references are analogous art and in the same field of endeavor, i.e., solving the problem of cache coherency and increasing bus bandwidth in a cache system.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al (US 5,627,993) and Lai (US 5,564,035).

As per claim 1, Abato discloses a data processing system comprising:

a system bus (bus 34; Fig. 1);

a processor with a level one cache memory responsively coupled to a level two cache memory which is responsively coupled via said system bus to a level three cache memory which is directly coupled to at least one memory storage (L1 cache 18 coupled to L2 cache 16 coupled via bus 34 to L3 cache 42 directly coupled to main memory 36; Fig. 1);

a circuit for directly snooping said system bus (column 8, lines 2-14).

However, Abato does not specifically teach a first logic which invalidates a corresponding level one cache memory location in response to either a non-local write request generated by another processor as recited in the claim.

Lai discloses a system wherein when a second processor performs write to memory, if there is a hit in L1 cache, corresponding cache line can be invalidated (col. 2, lines 41-57) to maintain multiprocessor coherency.

Since the technology for implementing invalidating a corresponding level one cache memory location in response to a non-local write was well known and since invalidating a corresponding level one cache memory location in response to a non-local write maintains multiprocessor coherency, an artisan would have been motivated to implement invalidating a corresponding level one cache memory location in response to a non-local write in the system of Abato.

Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Abato to include invalidating a corresponding level one cache memory location in response to a non-local write because it was well known to maintain multiprocessor coherency as taught by Lai.

8. Claim 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al (US 5,627,993) and Lai (US5,564,035) and Lynch et al. (US6,061,766).

As per claim 2, the combination of Abato and Lai does not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership as recited in the claim.

Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership [*snoop requests checks for the presence of an object in on-chip cache; only requests for exclusive use which match cache tags are invalidated; there is no invalidate done when there is no hit*; Fig. 4; col. 4, lines 19-30; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*] to provide a snoop process for ensuring cache coherency (col. 2, lines 34). Note that mode 3 requests without ownership is described as meaning that there is no data within the level one cache memory to invalidate.

Since the technology for implementing inhibiting a logic from invalidating mode 3 requests without ownership was well known and since inhibiting invalidating mode 3 requests without ownership provides a snoop process for ensuring cache coherency, an artisan would have been motivated to implement inhibiting invalidating mode 3 requests without ownership in the system of Abato and Lai.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Abato and Lai and Lynch before him at the time the invention was made, to modify the system of Abato and Lai to include implementing inhibiting a logic from invalidating mode 3 requests without ownership because it was well known to provide a snoop process for ensuring cache coherency as taught by Lynch.

As per claim 3, the combination of Abato and Lai does not specifically teach third logic which invalidates said corresponding cache memory location in response to a SNOOP hit as recited in the claim.

Lynch discloses invalidating a corresponding cache memory location in response to a SNOOP hit [Fig. 4; column 4, lines 24-26; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*] to provide a snoop process for ensuring cache coherency (column 2, lines 34).

Since the technology for implementing invalidating a corresponding cache memory location in response to a SNOOP hit was well known and since invalidating a corresponding cache memory location in response to a SNOOP hit provides a snoop process for ensuring cache coherency, an artisan would have been motivated to implement invalidating a corresponding cache memory location in response to a SNOOP hit in the system of Abato and Lai.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Abato and Lai and Lynch before him at the time the invention was made, to modify the system of Abato and Lai to include invalidating a corresponding cache

memory location in response to a SNOOP hit because it was well known to provide a snoop process for ensuring cache coherency as taught by Lynch.

As per claim 4, Lai discloses recording location of data in response to a level one cache read miss and a level two cache memory read miss to maintain multiprocessor coherency (col. 6, line 45 – col. 7, line 11).

Since the technology for implementing recording location of data in response to a level one cache read miss and a level two cache memory read miss was well known and since recording location of data in response to a level one cache read miss and a level two cache memory read miss maintains multiprocessor coherency, an artisan would have been motivated to implement recording location of data in response to a level one cache read miss and a level two cache memory read miss in the system of Abato.

Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Abato to include recording location of data in response to a level one cache read miss and a level two cache memory read miss because it was well known to maintain multiprocessor coherency as taught by Lai.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al (US 5,627,993) and Lynch et al. (US 6,061,766) and Lai (US 5,564,035) and Hazawa (US 4,891,809).

As per claim 5, the combination of Abato and Lai and Lynch discloses the claimed invention as detailed above in the previous paragraphs. However, Abato and Lai and Lynch do not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error to avoid loss of control between said level one cache memory and said level two cache memory as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col.3, lines 38-48]. Note that parity check is often used to check the accuracy with which each byte is stored as is well known by those of ordinary skill in the art.

It would have been obvious to one of ordinary skill in the art, having the teachings of Abato and Lynch and Hazawa before him at the time the invention was made, to modify the system of Abato and Lynch to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it was well known to provide a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for

generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught by Hazawa.

10. Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al (US 5,627,993) and Lai (US 5,564,035) and Duncan et al (US 6,128,711).

Claim 6 is rejected using the rationale as for the rejection of claim 1 above.

However, Abato and Lai do not specifically teach a level two cache memory dedicated to the processor as recited in the claim.

Duncan discloses a processor chip 40 including a secondary cache 48 is included on-chip (Fig. 2; col. 6, lines 1323).

Since the technology for implementing a level-two cache on-chip was well known as evidenced by Duncan, an artisan would have been motivated to implement this feature in the system of Abato and Lai.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Abato and Lai and Duncan before him at the time the invention was made,

to modify the system of Abato and Lai to include a level two cache memory dedicated to a processor because a level two cache included on chip provides data to the respective instruction and data stores to reduce the time required to obtain data from external memory (col. 6, lines 20-23) as taught by Duncan.

As per claim 9, Abato does not specifically teach fourth logic which records location of data in response to a level one cache read miss and a level two cache memory read miss as recited in the claim.

Lai discloses recording location of data in response to a level one cache read miss and a level two cache memory read miss to maintain multiprocessor coherency (col. 6, line 65 – col. 7, line 11). Since the technology for implementing recording in a level one cache memory location of data in response to a level one cache read miss and a level two cache memory read miss was well known as evidenced by Lai, an artisan would have been motivated to implement this feature in the system of Abato.

Thus, It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Abato to include recording location of data in response to a level one cache read miss and a level two cache memory read miss because it was well known to maintain multiprocessor coherency and to maintain cache coherency between the primary cache and main memory (col. 4, lines 7-10) as taught by Lai.

11. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al (US 5,627,993) and Lai (US5,564,035) and Duncan et al (US 6,128,711) and Lynch et al. (US6,061,766).

As per claim 7, the combination of Abato and Lai and Duncan does not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership as recited in the claim.

Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership [*snoop requests checks for the presence of an object in cache; only requests for exclusive use which match cache tags are invalidated*; *there is no invalidate done when there is no hit*; Fig. 4; col. 4, lines 19-30; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow*; *clearly, the use of multiple logics is an inherent feature of any computer system*] to provide a snoop process for ensuring cache coherency (col. 2, lines 34). Note that mode 3 requests without ownership is described as meaning that there is no data within the level one cache memory to invalidate.

Since the technology for implementing inhibiting a logic from invalidating mode 3 requests without ownership was well known and since inhibiting invalidating mode 3 requests without ownership provides a snoop process for ensuring cache coherency, an

artisan would have been motivated to implement inhibiting invalidating mode 3 requests without ownership in the system of Abato and Lai and Duncan.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Abato and Lai and Duncan and Lynch before him at the time the invention was made, to modify the system of Abato and Lai and Duncan to include implementing inhibiting a logic from invalidating mode 3 requests without ownership because it was well known to provide a snoop process for ensuring cache coherency as taught by Lynch.

As per claim 8, the combination of Abato and Lai and Duncan does not specifically teach third logic which invalidates said corresponding cache memory location in response to a SNOOP hit from a write request by another processor as recited in the claim.

Lynch discloses invalidating a corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*] to provide a snoop process for ensuring cache coherency (col. 2, lines 34).

Since the technology for implementing invalidating a corresponding cache memory location in response to a SNOOP hit was well known and since invalidating a corresponding cache memory location in response to a SNOOP hit provides a snoop process for ensuring cache coherency, an artisan would have been motivated to implement invalidating a corresponding cache memory location in response to a SNOOP hit in the system of Abato and Lai and Duncan.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Abato and Lai and Duncan and Lynch before him at the time the invention was made, to modify the system of Abato and Lai and Duncan to include invalidating a corresponding cache memory location in response to a SNOOP hit because it was well known to provide a snoop process for ensuring cache coherency as taught by Lynch.

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al (US 5,627,993) and Lai (US 5,564,035) and Duncan et al (US 6,128,711) and Hazawa (US 4,891,809).

As per claim 10, the combination of Abato and Lai and Duncan discloses the claimed invention as detailed above in the previous paragraphs. However, Abato and

Lai and Duncan do not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col.3, lines 38-48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Abato and Lai and Duncan and Hazawa before him at the time the invention was made, to modify the system of Abato and Lai and Duncan to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it was well known to provide a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught y Hazawa.

13. Claims 11, 14, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai (US 5,564,035) and Duncan et al (US 6,128,711) and Arimilli et al (US 6,021,468).

As per claim 11, Lai discloses a method of maintaining validity of data within a semi store-in level one cache memory of a processor responsively coupled to a level

two cache memory which is responsively coupled to a system memory bus [*L1 cache 202, L2 cache 203, system bus 208*; Fig. 3] comprising: formulating a write request [*processor 210 performs a write to memory*; col. 2, lines 48-49]; first checking for a level one cache memory hit in response to said write memory request [*hit in L1 cache 202*; col. 2, lines 48-52; col. 1, lines 60-62]; second checking a level two cache memory hit in response to a hit found by said first experiencing step [*L2 cache 203 detects a hit*; col. 2, lines 48-49; col. 2, lines 35-37]; and invalidating a portion of said level one cache memory corresponding to said write memory request in response to a hit found by said second checking step [*hit in L1 cache corresponding cache line can be invalidated*; col. 2, lines 52-57].

However, Lai does not specifically teach a level-two cache dedicated to a processor as recited in the claim.

Duncan discloses a processor chip 40 including a secondary cache 48 is included on-chip (Fig. 2; col. 6, lines 13-23).

Since the technology for implementing a level-two cache on-chip was well known as evidenced by Duncan, an artisan would have been motivated to implement this feature in the system of Lai.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Lai and Duncan before him at the time the invention was made, to modify

the system of Lai to include a level two cache memory dedicated to a processor because a level two cache included on chip provides data to the respective instruction and data stores to reduce the time required to obtain data from external memory (col. 6, lines 20-23) as taught by Duncan.

However, the combination of Lai and Duncan do not specifically teach a semi-store-in cache as recited in the claim.

Arimilli discloses a system wherein a store-in cache can be used to effectively increase bus bandwidth (column 5, lines 46-51).

Regarding claim 11, it would have been obvious to one of ordinary skill in the art, having the teachings of Lai and Duncan and Arimilli before him at the time the invention was made, to modify the system of Lai and Duncan to include a semi-store-in level one cache because it was well know to provide the advantage of effectively increasing bus bandwidth (column 5, lines 46-51) as taught by Arimilli.

As per claim 14, Lai discloses recording location of data in response to a level one cache read miss and a level two cache memory read miss to maintain multiprocessor coherency (col. 6, line 65 – col. 7, line 11).

As per claim 16, Lai discloses an apparatus comprising:

executing means for executing program instructions [*processor 200, 210*; Fig. 3]; level one caching means responsively coupled to said executing means for level one caching data [*L1 cache 202*; Fig. 3]; accessing means responsively coupled to said executing means and said level one caching means for accessing a data element if said executing means requires accessing of said data element [*system bus 208*; Fig. 3]; level two caching means responsively coupled to said requesting means for level two caching data [*L2 cache 203*; Fig. 3]; and first invalidating means responsively coupled to said level one caching means for invalidating said data element if said data element is a write data element located within said level two caching means and within said level one caching means [*hit in L2 cache and hit in L1 cache, corresponding cache line can be invalidated*; col. 2, lines 52-57].

However, Lai does not specifically teach a level-two cache dedicated to a processor as recited in the claim.

Duncan discloses a processor chip 40 including a secondary cache 48 is included on-chip (Fig. 2; col. 6, lines 13-23).

Since the technology for implementing a level-two cache on-chip was well known as evidenced by Duncan, an artisan would have been motivated to implement this feature in the system of Lai.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Lai and Duncan before him at the time the invention was made, to modify the system of Lai to include a level two cache memory dedicated to a processor because a level two cache included on chip provides data to the respective instruction and data stores to reduce the time required to obtain data from external memory (col. 6, lines 20-23) as taught by Duncan.

However, the combination of Lai and Duncan do not specifically teach a semi-store-in cache as recited in the claim.

Arimilli discloses a system wherein a store-in cache can be used to effectively increase bus bandwidth (column 5, lines 46-51).

Regarding claim 16, it would have been obvious to one of ordinary skill in the art, having the teachings of Lai and Duncan and Arimilli before him at the time the invention was made, to modify the system of Lai and Duncan to include a semi-store-in level one cache because it was well know to provide the advantage of effectively increasing bus bandwidth (column 5, lines 46-51) as taught by Arimilli.

As per claim 19, Lai discloses recording location of data in response to a level one cache read miss and a level two cache memory read miss to maintain multiprocessor coherency [col. 6, line 45 – col. 7, line 11].

14. Claims 12-13 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai (US 5,564,035) and Duncan et al (US 6,128,711) and Arimilli et al (US 6,021,468) and Lynch et al. (US 6,061,766).

As per claims 12 and 17, Lai and Duncan and Arimilli do not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership as recited in the claim.

Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership [*snoop requests checks for the presence of an object in cache; only requests for exclusive use which match cache tags are invalidated*; *there is no invalidate done when there is no hit*; Fig. 4; col. 4, lines 19-30; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow*; *clearly, the use of multiple logics is an inherent feature of any computer system*] to provide a snoop process for ensuring cache coherency (col. 2, lines 34).

Since the technology for implementing inhibiting a logic from invalidating mode 3 requests without ownership was well known and since inhibiting invalidating mode 3

requests without ownership provides a snoop process for ensuring cache coherency, an artisan would have been motivated to implement inhibiting invalidating mode 3 requests without ownership in the system of Lai and Duncan and Arimilli.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Lai and Duncan and Arimilli and Lynch before him at the time the invention was made, to modify the system of Lai to include implementing inhibiting a logic from invalidating mode 3 requests without ownership because it was well known to provide a snoop process for ensuring cache coherency as taught by Lynch.

As per claims 13 and 18, the combination of Lai and Duncan and Arimilli do not specifically teach third logic which invalidates said corresponding cache memory location in response to a SNOOP hit as recited in the claim.

Lynch discloses invalidating a corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*] to provide a snoop process for ensuring cache coherency (col. 2, lines 34).

Since the technology for implementing invalidating a corresponding cache memory location in response to a SNOOP hit was well known and since invalidating a

corresponding cache memory location in response to a SNOOP hit provides a snoop process for ensuring cache coherency, an artisan would have been motivated to implement invalidating a corresponding cache memory location in response to a SNOOP hit in the system of Lai and Duncan and Arimilli.

Thus, it would have been obvious to one of ordinary skill in the art, having the teachings of Lai and Duncan and Arimilli and Lynch before him at the time the invention was made, to modify the system of Lai to include invalidating a corresponding cache memory location in response to a SNOOP hit because it was well known to provide a snoop process for ensuring cache coherency as taught by Lynch.

15. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lai (US 5,564,035) and Duncan et al (US 6,128,711) and Arimilli et al (US 6,021,468) and Hazawa (US 4,891,809).

As per claims 15 and 20, the combination of Lai and Duncan and Arimilli and Lynch discloses the claimed invention as detailed above in the previous paragraphs. However, Lai and Duncan and Arimilli and Lynch do not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error (column 3, lines 38-48).

It would have been obvious to one of ordinary skill in the art, having the teachings of Lai and Duncan and Arimilli and Hazawa before him at the time the invention was made, to modify the system of Lai to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it was well known to provide a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit (col. 1, lines 30-37) as taught y Hazawa.

16. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al (US 5,627,993) and Hazawa (US 4,891,809).

Claim 21 is rejected using the rationale as for the rejection of claim 1 above.

However, Abato does not specifically teach a data element having a parity error stored in said level two cache memory and a facility responsively coupled to said level one cache memory and said level two cache memory which detects said parity error of

said data element and invalidates a corresponding data element within said level two cache memory as recited in the claim.

Hazawa discloses invalidating data in a level two cache memory in response to a parity error of a data element to provide a cache memory with an error checking mode column 3, lines 38-51; column 3, lines 38-59).

It would have been obvious to one of ordinary skill in the art, having the teachings of Abato and Hazawa before him at the time the invention was made, to modify the system of Mayfield to include invalidating data in a level two cache memory in response to a parity error of a data element because it was well known to provide a cache memory having a normal error checking mode as taught by Hazawa.

17. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al (US 5,627,993) and Hazawa (US 4,891,809) and Lynch et al (US 6,061,766).

As per claim 22, the combination of Abato and Hazawa discloses the claimed invention as detailed above in the previous paragraphs. However, Abato and Hazawa do not specifically teach a level one cache memory comprising a level one instruction cache memory and a level one operand cache memory as recited in the claim.

Lynch discloses a level one cache comprising a data cache for storing data as it is passed back and forth from the execution units of the processor and an instruction cache holding instructions prior to execution by the processor's execution units (col. 3, lines 43-48).

It would have been obvious to one of ordinary skill in the art, having the teachings of Abato and Hazawa and Lynch before him at the time the invention was made, to modify the system of Abato and Hazawa to include a level one instruction cache memory and a level one operand cache memory because a level one data cache was well known for storing data as it is passed back and forth from the execution units of the processor and a level one instruction cache was well known for holding instructions prior to execution by the processor's execution units as taught by Lynch.

18. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abato et al (US 5,627,993) and Hazawa (US 4,891,809) and Lynch et al (US 6,061,766) and Lai (US 5,564,035).

As per claim 23, the combination of Abato and Hazawa and Lynch discloses the claimed invention as detailed above in the previous paragraphs. However, Abato and Hazawa and Lynch do not specifically teach invalidating a write data element of a level

one cache memory in response to a level one cache memory write hit and a level two cache memory hit as recited in the claim.

Lai discloses invalidating a write data element of a level one cache memory in response to a level one cache memory write hit and a level two cache memory hit [*hit in L2 cache and hit in L1 cache, corresponding cache line can be invalidated*; col. 2, lines 41-57] to maintain multiprocessor coherency.

Since the technology for implementing invalidating a corresponding level one cache memory location in response to a level one write hit and a level two write hit was well known and since invalidating a corresponding level one cache memory location in response to a level one write hit and a level two write hit maintains multiprocessor coherency, an artisan would have been motivated to implement invalidating a corresponding level one cache memory location in response to a level one write hit and a level two write hit in the system of Abato and Hazawa.

Thus, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Abato and Hazawa to include invalidating a corresponding level one cache memory location in response to a level one write hit and a level two write hit because it was well known to maintain multiprocessor coherency and to maintain cache coherency between the primary cache and main memory (col. 4, lines 7-10) as taught by Lai.

As per claim 24, Lynch discloses a snooping circuit [*snoop queue 402*; Fig. 4].

As per claim 25, Lynch discloses said write data element is located within said level one operand cache memory [col. 3, lines 43-45].

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

20. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

21. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (571) 272-4215. The examiner can normally be reached on 8:30 am - 6:00 pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 31, 2005

PIERRE VITAL
PRIMARY EXAMINER